What is claimed is:

1. A calculation system of fault coverage comprising:

a data acquiring module configured to acquire layout information and gate net data of an LSI;

a layout analysis and fault link module configured to analyze a condition of connection of an input terminal and an output terminal of a basic cell regarding an entire layout based on the layout information and the gate net data, to extract the result of the analysis as layout element information, and to generate an undetected fault list;

a fault detecting module configured to execute any of fault simulation and an automatic test pattern generation on the undetected fault list and to generate a detected and undetected fault list; and

a weight calculating module configured to add the layout element information corresponding to a fault in the detected and undetected fault list as weight, based on a link file between faults and layout element information to be generated based on the layout information, the gate net data, and the detected and undetected fault list by the layout analysis and fault link module.

2. The system of claim 1, wherein the layout analysis and fault link module comprising:

a net information extractor configured to extract net information from the layout information and the gate net data;

a path extractor configured to extract a path connecting between the basic cells from the layout information and the gate net data;

a detected time information extractor configured to extract information indicating that faults assumed to occur on the input terminal and on the output terminal are detected at the same time from the detected and undetected fault list;

a fault list generator configured to generate a fault list from the layout information and the gate net data; and

a fault linker configured to generate a link file between faults and layout element information by linking the layout information, the gate net data, and the detected and undetected fault list.

3. The system of claim 1, wherein the weight calculating module comprise:

a total layout element calculator configured to calculate total layout elements of net information except the part that redundant fault influenced; and

a weight calculator configured to calculate weighted pin stuck-at fault coverage based on a link file between faults and layout element information, and to generate a weighted undetected fault list.

4. The system of claim 3, wherein the weighted pin stuck-at fault coverage and the weighted undetected fault list includes:

wire length weighted fault coverage and a wire length weighted undetected fault list;

number of vias weighted fault coverage and a number of vias weighted undetected fault list;

basic cell area weighted fault coverage and a basic cell area weighted undetected fault list; and

suitably weighted fault coverage and a suitably weighted undetected fault list.

5. The system of claim 4, wherein the wire length weighted fault coverage is calculated by dividing a wire length corresponding to the detected faults by an evaluated total wire length except the part that redundant faults influenced.

6. The system of claim 4, wherein the number of vias weighted fault coverage is calculated by dividing a number of vias corresponding to the detected faults by an evaluated total number of vias except the part that redundant faults influenced.

7. The system of claim 6, wherein the number of vias weighted fault coverage is calculated by counting a number of minimum vias, a number of double vias and a number of stacked vias at the suitable ratio respectively.

8. The system of claim 4, wherein the basic cell area weighted fault coverage is calculated by dividing a basic cell area corresponding to the detected faults by an evaluated total basic cell area except the part that redundant faults influenced.

9. The system of claim 1, wherein the fault detecting module comprises at least any of the fault simulator and the automatic test pattern generation.

10. The system of claim 2, wherein the layout analysis and fault link module further comprising a layout element information extractor configured to extract basic cell layout element information from basic cell details layout data.

11. A computer-implemented calculation method of fault coverage comprising:

acquiring layout information and gate net data of an LSI;

generating a fault list by analyzing a condition of connection of an input terminal and an output terminal of a basic cell regarding an entire layout based on the layout information and the gate net data and extracting the result of the analysis as layout element information;

executing any of fault simulation and automatic test pattern generation on the fault list and generating a detected and undetected fault list;

generating a link file between faults and layout element information by use of the layout information, the gate net data, and the detected and undetected fault list; and

adding a layout element corresponding to any one of a detected fault and a undetected fault as weight.

12. The method of claim 11, wherein the generating the link file between faults and layout element information comprises:

extracting a path connecting between the basic cells from the layout information and the gate net data;

extracting information indicating that faults assumed to have

occurred on the input terminal and on the output terminal are detected at the same time from the detected and undetected fault list; and

generating a link file between faults and layout element information by linking the layout information, the gate net data, and the information indicating that faults assumed to have occurred on the input terminal and on the output terminal are detected at the same time.

13. The method of claim 11, wherein the adding the layout element comprises:

calculating total layout elements of the connection wiring except the part that redundant faults influenced; and

repeating addition of a corresponding layout region and a layout element to any of the input terminal and the output terminal based on the link file between faults and layout element information when a path is activated in response to the detected fault and the undetected fault, calculating weighted pin stuck-at fault coverage, and generating a weighted undetected fault list.

14. The method of claim 12, wherein the weighted pin stuck-at fault coverage and the weighted undetected fault list are any of wire length weighted fault coverage and a wire length weighted undetected fault list, and number of vias weighted fault coverage and a number of vias weighted undetected fault list, and basic cell area weighted fault coverage and a basic cell area weighted undetected fault list, and suitably weighted fault coverage and a suitably weighted undetected fault list.

15. The method of claim 14, wherein the wire length weighted fault coverage is calculated by dividing a wire length corresponding to the detected fault by an evaluated total wire length except the part that redundant faults influenced.

16. The method of claim 14, wherein the number of vias weighted fault coverage is calculated by dividing a number of vias corresponding to the detected fault by an evaluated total number of vias except the part that redundant faults influenced.

17. The method of claim 16, wherein the number of vias weighted fault coverage is calculated by counting a number of minimum vias, a number of double vias and a number of stacked vias at the suitable ratio respectively.

18. The method of claim 14, wherein the basic cell area weighted fault coverage is calculated by dividing a basic cell area corresponding to the detected fault by an evaluated total basic cell area except the part that redundant faults influenced.

19. The method of claim 11, wherein the detected and undetected fault list is generated by executing any of fault simulation and an automatic test pattern generation.

20. The method of claim 12, wherein the generating the link file between faults and layout element information further comprising extracting a basic

cell layout element information from the a basic cell details layout data.